library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

entity Bist\_D is

port(

M : in BIT;

D : in BIT;

Q : buffer BIT;

NQ : buffer BIT

);

end Bist\_D;

--}} End of automatically maintained section

architecture Arhitectura of Bist\_D is

signal s1,s2,clock:bit;

begin

-- enter your statements here --

clk: process -- Generator semnal de tact

begin

clock<='0';

wait for 100 ns;

clock<='1';

wait for 100 ns;

end process clk;

n1:process(m)

begin

s1<=not(m);

end process n1;

nand1:process(s1,clock)

begin

s2<=s1 nand clock;

end process nand1;

d1:process(s2)

begin

if s2='1' then

q<=d;

nq<=not(d);

end if;

end process d1;

end Arhitectura;